CLAIMS:

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1. A computer processor, comprising:

a plurality of processing units; and

communication means by which the plurality of processing units are interconnected,

wherein said communication means is dynamically configurable based on a computer program to be processed such that the processing units can selectively be arranged in at least first and second distinct configurations, the first distinct configuration has a larger number of the processing units arranged in parallel than the second distinct configuration, and the second distinct configuration has a deeper pipeline depth than the first distinct configuration.

2. A computer processor according to claim 1 wherein said communication means forms logical connections between said processing units and said first and second configurations comprise logical configurations.

3. A computer processor according to claim 1, wherein said communication means includes a data bus configurable to selectively interconnect the processing units into at least the first and second distinct configurations.

4. A computer processor according to claim 3, wherein each of the processing units includes control means for selecting one of a plurality of data reception and transmission modes, the first and second distinct configurations being selectable by altering a control

signal provided to each control means by an instruction controller associated with said computer processor.

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5. A computer processor according to claim 3, wherein the data bus is a packet-based bus and each of said processing units is adapted to place data on and take data from the packet-based bus, the first and second configurations being selectable by manipulating packet addressing on the packet-data bus.

6. A computer processor according to claim 1, wherein program instruction included in the computer program are provided to said processing units in a variable length Very Long Instruction Word (VLIW) format, the configuration of said computer processor being dynamically selected based upon the length of the VLIW.

7. A computer processor according to claim 6, wherein the configuration of said computer processor is executed in accordance with a program compiler.

8. A computer processor according to claim 1, wherein subject data to be processed by said computer processor includes image data, and the first configuration is used for processing the image data whilst the second configuration is used for processing other data included in the subject data.

9. A computer processor according to claim 1, wherein subject data to be processed by the computer processor includes image data, the first configuration is used for executing a first type of image processes having no necessity for feed-forward of data

calculations whilst the second configuration is used for executing a second type of image processes having a necessity for feed-forward of data calculations.

10. A computer processor according to claim 9, wherein said first type of image processes comprises one of graphic composition, colour space conversion and convolution, and said second type of image processes comprises one of filtering and error diffusion.

11. A method of data processing using a computer processor having a plurality of processing units interconnected by communication means, said method comprising the step of:

dynamically configuring said communication means according to on a computer program to be processed such that said processing units are selectively arranged in a plurality of configurations having a different number of said processing units arranged in parallel and a different number of said processing units arranged in pipelined layers .

12. A method according to claim 11, wherein subject data to be processed by the computer processor includes image data, and a configuration used for processing the image data has a larger number of said processing units arranged in parallel and a smaller number of pipelined layers than a configuration used for processing other data included in the subject data.

13. A method according to claim 11, wherein subject data to be processed by the computer processor includes image data, and a configuration used for executing a first type of image processes having no necessity for feed-forward of data calculations has a

larger number of said processing units arranged in parallel and a smaller number of pipelined layers than a configuration used for executing a second type of image processes having a necessity for feed-forward of data calculations.

14. A method according to claim 13, wherein said first type of image processes includes one of graphic composition, colour space conversion and convolution, and said second type of the image processes includes one of filtering and error diffusion.

15. A computer processor according to claim 1 wherein said processing units each comprise an SIMD arrangement.

16. A computer processor according to claim 15 wherein data to be processed by said computer processor comprises image data and said computer processor comprises at least one said SIMD arrangement for each colour component of said image data.